Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application. Where claims have been amended and/or canceled, such amendments and/or cancellations are done without prejudice and/or waiver and/or disclaimer to the claimed and/or disclosed subject matter, and the applicant and/or assignee reserves the right to claim this subject matter and/or other disclosed subject matter in a continuing application.

Listing of Claims:

Claims 1-23 (Canceled)

24. (New): An apparatus, comprising:

means for determining if at least a portion of an instruction is stored in a loop buffer; and

means for determining if at least a portion of the instruction is stored in a cache;

said means for determining if at least a portion of the instruction is in a loop buffer comprising means for determining if at least a portion of the instruction is in first portion of a memory array, and said means for determining if at least a portion of the instruction is in the cache comprising means for determining if at least a portion of the instruction is in a second portion of the memory array.

25. (New): An apparatus as claimed in claim 24, said means for determining if at least a portion of the instruction is in a loop buffer comprising means for determining if at least a portion of an address corresponding to the instruction is substantially equal to a tag address.

26. (New): An apparatus as claimed in claim 24, said means determining if at least a potion of the instruction is in a loop buffer comprising means for comparing at least a potion of an address corresponding to the instruction with at least a portion of a logic value stored in a tag register.

27. (New): An apparatus as claimed in claim 24, said means for determining if at least a portion of the instruction is in a loop buffer comprising means for determining if at least a portion of the instruction is in first portion of a memory array, and said means for determining if at least a portion of the instruction is in the cache comprising means for determining if at least a portion of the instruction is in a second portion of the memory array, the first portion of the memory array being substantially contiguous with the second portion of the memory array.

28. (New): An apparatus as claimed in claim 24, further comprising means for loading a tag register after said means for determining if at least a portion of the instruction is stored in a cache determines at least a portion of the instruction is in the cache.

29. (New): An apparatus as claimed in claim 28, said means for loading the tag register comprising means for loading a logic value that corresponds at least in part to a storage location in a memory array.

30. (New): An apparatus as claimed in claim 29, further comprising means for determining if at least a portion of an additional instruction is in a loop buffer, and means for determining if at least a portion of the additional instruction corresponds to the logic value in the tag register.

31. (New): An apparatus, comprising:

a memory array comprising a loop buffer and a cache;

means for determining if a first piece of data is in the loop buffer;

means for enabling a portion of the memory array corresponding to the loop buffer; and

means for determining if a second piece of data is in the cache if the second piece of data is not in the loop buffer.

32. (New): An apparatus as claimed in claim 31, said means for enabling a portion of the memory array comprising means for enabling only the portion of the memory array comprising the first piece of data.

33. (New): An apparatus as claimed in claim 31, further comprising:

means for enabling the memory array if the second piece of data is not in the loop buffer.

34. (New): An apparatus as claimed in claim 31, further comprising:

means for loading a tag register with a first logic value corresponding, at least in part, to a location of the second piece of data in the memory array.

35. (New): An apparatus as claimed in claim 34, further comprising:

means for determining if a third piece of data is stored in the loop buffer and means for determining if the first logic value stored in the tag register corresponds, at least in part, to the third piece of data.

36. (New): An apparatus as claimed in claim 35, further comprising:

means for determining if the third piece of data is in the memory array if the third piece of data is not in the loop buffer; and

means for loading the tag register with a second logic value corresponding, at least in part, to a location of the third piece of data in the memory array.

27. (New): An apparatus as claimed in claim 36, said means for loading the tag register with the second logic value comprises means for loading the tag register with a logic value that is different than the first logic value.

38. (New): An apparatus as claimed in claim 31, said means for determining if the second piece of data is in the cache comprises means for determining if the second piece of data is in the memory array.

39. (New): An apparatus as claimed in claim 31, further comprising:

means for disabling a tag look-up of the memory array.

40. (New): An apparatus as claimed in claim 31, further comprising:

means for providing at least a portion of the first piece of data to a digital signal processing core.